WHAT IS CLAIMED IS:

1. A semiconductor wafer fabricating method, comprising the steps of:

setting, to a power supply for supplying an output of a current, a voltage, or power as an output item necessary for processing of a semiconductor wafer, strength of the output item;

setting outputting of the output item to "on" or "off";

sensing the output item and providing an output sense signal according to a value obtained by sensing the output item; and

stopping the processing for a subsequent semiconductor wafer to be processed in response to an event in which the output sense signal exceeds a predetermined threshold value when the outputting of the output item is "off".

2. A semiconductor wafer fabricating method, comprising the steps of:

setting, to a power supply for supplying a current, a voltage, or power as an output item necessary for processing of a semiconductor wafer, a strength of the output item;

setting outputting of the output item to "on or off;

sensing the output item to provide an output sense signal according to a value obtained by sensing the output item; and

assuming occurrence of an abnormality and displaying an abnormality indication in response to an event in which the output sense

signal exceeds a predetermined threshold value when the outputting of the output item is "off".

3. A semiconductor wafer fabricating method for use with power supply for supplying power indicating a current or a voltage necessary for processing a semiconductor wafer, comprising the steps of:

setting a strength of the power to a predetermined value;

setting the supply of the power to "on" or "off";

sensing the power presently being supplied to the semiconductor wafer processing and outputting a sense signal according to a value obtained by sensing the present power;

sensing the power when a power state is set "off", determining occurrence of an abnormality when the sense signal according to a value obtained by sensing the power exceeds a predetermined value, and generating an abnormality occurrence signal indicating occurrence of the abnormality; and

inhibiting, in response to the abnormality occurrence signal, the processing for a subsequent semiconductor wafer to be processed.